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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,404	07/11/2003	Steven P. Young	X-1392 US	5533

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,404	YOUNG, STEVEN P.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *30 and 31* is/are allowed.

6)☒ Claim(s) *1-7,21-29 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-11-03,10-14-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, claims 1-7 and 21-32 in the reply filed on 11-9-2004 is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Regarding claims 1-4, the phrase "column-like are" renders the claim(s) indefinite because the claim(s) include(s) elements not actually disclosed (those encompassed by "or the like"), thereby rendering the scope of the claim(s) unascertainable. See MPEP § 2173.05(d).

Claim Objections

Claim 32 is objected to because of the following informalities: "a input/output" on line 3 appears to be --an input/output--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-7, 21-24 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Seefeldt et al. (US PAT No. 4,978,633).

Regarding claim 1, Fig. 2 of Seefeldt et al. teaches an integrated circuit (IC) having programmable interconnections (41; col. 2, lines 5-18), comprising: a first plurality of regions (31, 32), each region having a programmable circuit with a programmable function (col. 2, lines 21-29); and a second plurality of column areas (6 columns of 32, 31) of the IC, wherein each column area of the second plurality extends from one edge of the IC to an opposing edge of the IC (col. 2, lines 30-49), and wherein each column area of the second plurality comprises predetermined regions of the first plurality (each column has 31 and 32), wherein the predetermined regions in a column area substantially fill the column area and wherein each of the predetermined regions in the column area comprises programmable circuits substantially identical to programmable circuits in at least two other predetermined regions in the column area (two middle columns has the substantially identical to each other).

Regarding claim 2, Fig. 2 of Seefeldt et al. teaches the integrated circuit of claim 1 wherein every predetermined region in the predetermined regions in the column area has a circuit of only one circuit type (the second columns from the left and right edge has only GATE which is super logic function cell), the circuit type selected from a group consisting of Configurable Logic Block (CLBs), Multi-Giga Bit Transceivers (MGTs), Block Random Access Memories IBRAMs), Digital Signal Processor (DSP) circuits, Multipliers, and Input/output Blocks (IOBs).

Regarding claim 4, Fig. 2 of Seefeldt et al. teaches the integrated circuit of claim 1 further comprising a heterogeneous column area of the IC, the heterogeneous column area having regions with programmable circuits that are of different circuit types (I/O or GATE).

Regarding claim 5, Fig. 2 of Seefeldt et al. teaches a die having an integrated circuit, comprising: a first set of regions (I/O supercells), each region in the first set having an Input/Output circuit (Fig. 3 shows I/O circuit), a second set of regions (GATE supercell), each region in the second set having a circuit with a programmable logic function (supercell is configurable to perform a signal processing operation; ABSTRACT); a third set of columns (set of columns in Fig. 2), wherein a top of each column of the third set is positioned at a top side of the die and a bottom of each column of the third set is positioned at a bottom side of the die (top and bottom sides of columns); a first column of the third set consisting essentially of regions from the first set (left-most column in Fig. 2 is a column essentially of I/O supercells); and a second column of the third set (column right next to the left-most column is a column essentially of super gate cell) consisting essentially of regions from the second set, wherein the second column is interposed between the first column and a nearest side edge of the die (the second column is positioned between the left-most column and the right-most column; size of array is not fixed, col. 5, lines 50-61).

Regarding claim 6, Fig. 2 of Seefeldt et al. teaches the die of claim 5 wherein an Input/Output circuit comprises a Multi-Giga Bit Transceiver or an input/output block or a combination thereof (Fig. 3 discloses an input/output circuit).

Regarding claim 7, Fig. 2 of Seedfeldt et al. teaches the die of claim 5 further comprising a third column of the third set positioned at a center line of the die, the third set comprising assorted tiles (the third column and the fourth column from the left side is positioned at a center line with I/O supercells and GATE supercells).

Regarding claim 21, Fig. 2 of Seedfeldt et al. teaches a method, comprising: providing a plurality of configurable logic blocks in a column, the column extending from a first side of an integrated circuit die to a second side of the integrated circuit die (six columns of supercells extending from a top side to a bottom side).

Regarding claim 22, Fig. 2 of Seedfeldt et al. teaches the method of Claim 21, further comprising: providing a first input/output block on a first side of the column (top side of the left-most column has I/O supercell); and providing a second input/output block on a second side of the column (bottom side of the left-most column has I/O supercell).

Regarding claim 23, Fig. 2 of Seedfeldt et al. teaches the method of Claim 22, wherein there is no input/output block disposed between the column of configurable

logic blocks and the first side of the integrated circuit die, and wherein there is no input/output block disposed between the column of configurable logic blocks and the second side of the integrated circuit die (the second column from the left has only GATE supercells with no I/O supercell between the top side and the bottom side).

Regarding claim 24, Fig. 2 of Seedfeldt et al. teaches the method of Claim 21, wherein the column includes the plurality of configurable logic blocks as well as a plurality of clock distribution tiles (the third column from the left has GATE supercells as well as I/O cells where I/O cells is used for signal, e.g. clock distribution).

Regarding claim 32, Fig. 2 of Seefeldt et al. teaches an integrated circuit consisting essentially of tiles (supercells), the integrated circuit comprising an input/output block tile (I/O supercell in the third column and third row surrounded by other supercells) having four sides where the input/output block tile is bounded on each of the its four sides by another tile.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seefeldt et al. in view of Cory et al. (US PAT No. 6,617,877).

Regarding claim 3, Fig. 2 of Seefeldt et al. teaches the integrated circuit of claim 1 where a column area of the second plurality has predetermined regions comprising Gate supercells and I/O supercells, but does not disclose a column area having predetermined regions comprising Multi-Giga Bit Transceiver circuits. However, Fig.1 of Cory et al. teaches a multi-gigabit transceivers (MGT) included in a PLD for the purpose of optimizing the data paths between the core logic of a PLD and the MGTs located on the PLD. Therefore it would have been obvious at the invention was made to a person ordinary skill in the art to utilize the MGT of Cory et al. in the Gate supercells and I/O supercells of Seefeldt et al. to provide data path optimization.

Claims 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seefeldt et al..

Regarding claims 25 and 26, Fig. 2 of Seefeldt et al. teaches the method of claim 21 where the area of the column is occupied by input/output blocks (I/O supercells) and configurable logic blocks (Gate supercells) where the I/O supercells and Gate supercells are dispersed in order to obtain better routability (col. 6, lines 12-23), and an integrated circuit having a but does not disclose the specific value of ratio of I/O supercells and Gate supercells being over ninety-five percent of the die area. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the specific value of ration being over 95% since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable

value or ranges of an effective variable involves only routine skill in the art (see In re Boesch, 617 F2d 272, 205 USPQ 215(CCPA 1980) and In re Aller, 105 USPQ 233).

Regarding 27, Fig. 2 of Seefeldt et al. teaches the integrated circuit of claim 26 where each of the input/output block tiles in the column has an identical layout (Fig. 3 shows topology for I/O supercells used in Fig. 2).

Regarding claim 28, Fig. 2 of Seefeldt et al. teaches the integrated circuit of claim 26 where the integrated circuit is a field programmable gate array (a gate array of supercells programmable, col. 3, lines 11-42).

Regarding claim 29, Fig. 2 of Seefeldt et al. teaches the integrated circuit of Claim 26, wherein the integrated circuit is disposed on a semiconductor die, the semiconductor die having a first side (top), a second side (bottom) opposite the first side, a third side (left), and a fourth side (right) opposite the third side, and wherein the column of tiles extends from the first side and to the second side (left-most column extends from the top to bottom), a first input/output block tile of the column (top I/O on the left-most column is adjacent to the top side) being disposed adjacent the first side of the die, a second input/output block tile of the column (bottom I/O on the left-most column is adjacent to the bottom side) being disposed adjacent the second side of the die.

Allowable Subject Matter

Claims 30-31 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance: one of ordinary skill in the art would not have been motivated to modify the teaching of Seefeldt et al. and/or Cory et al. to further includes, among other things, the specific of input/output block tiles disposed in columns where each of the columns extending in a first direction, where no two input/output block tiles of the integrated circuit are disposed adjacent to one another to form a row that extends in a second direction perpendicular to the first direction, as set forth in the claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Schultz (US PAT No. 6,781,407) discloses FPGA and embedded circuitry initialization and processing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

Date: 12-28-2004